**Procedure for running the Xilinx simulation**

The verhilog code for written 4x16 decoder using two 3x8 decoder using enable.

We had done it using module instantiations of the verhilog code i.e., we had written the verhilog code for a 3x8 decoder then we use the copy of this module in 4x16 decoder.

Steps to view the RTL view of the circuit:

Step 1:

In Xilinx to view the RTL view of the circuit, Click on the “Implementational” part of the code.

Step 2:

Then click on “Synthesize-XST” to run it. After that, click on “view RTL Schematic”.

Steps to see the timing diagram and for the simulation of the code:

Step 1:

Click on the simulate part of the Xilinx

Step 2:

Now select the file which you want to simulate.

Step 3:

Now create the test case file for the code.

Step 4:

Now click on “Behavioural check System” to simulate it.

Step 5:

After it gets completed, now click on “simulate Behavioural..”

Step 5:

Now the timing diagram will appear.

Step 6:

First applying the test benches, we get the correct output set for 4x16 decoder

Step 7:

To forcefully make a line stuck at 1 we will insert an OR gate at that position through our Verilog code. Then the line behave as stuck at 1 fault.

Step 8:

Now again applying the test bench we will get the output of the faulty decoder.

Step 9:

Now we will compare both the output set.

If the output of expected and actual truth table mismatches for the same input then that input set will be the test set of the corresponding fault position.

Example:

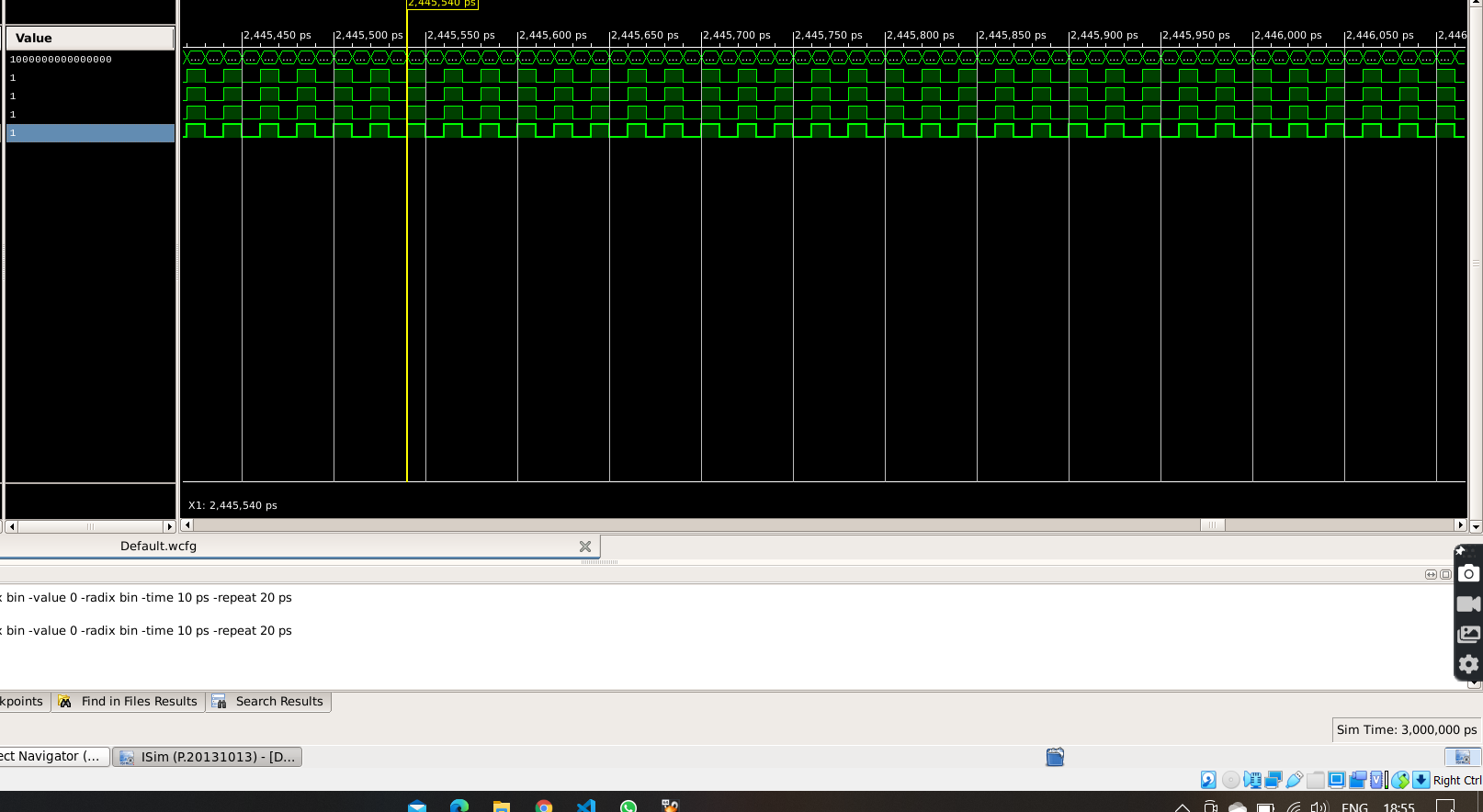


Figure: Normal timing diagram of the clock wise input.

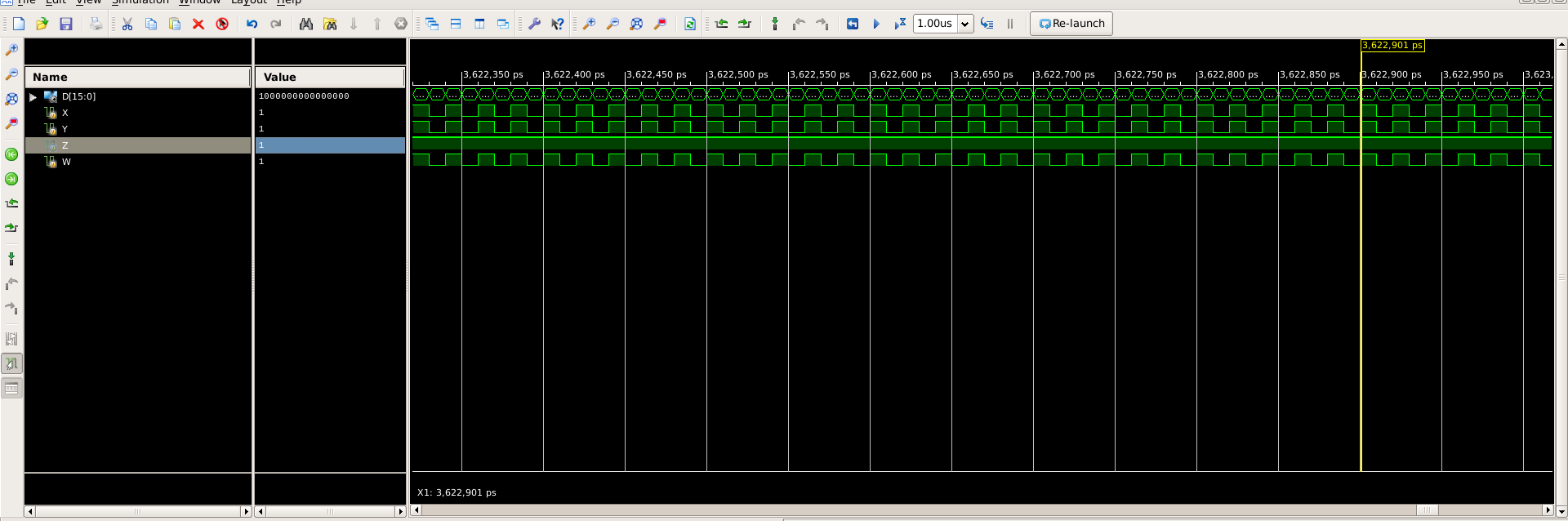


Figure: Timing Diagram when Input Z is forced to 1

**PROCEDURE TO SIMULATE IN WEBSITE**

1. First on the VCC.

(As the circuit in the simulation is faulty one based on single stuck at 1 fault model, so u will get unusual result)

1. Click on the “input” button to give the input.

Green-(Input 1)

Red -(Input 0)

1. After selecting input value, you will get the corresponding faulty output, to add the result in the truth table click on “ADD” button.
2. Repeat 2 and 3 to get all the faulty output at the current fault position.
3. Now compare it with the real truth table and try to get the fault position.
4. To change the fault position, click on “Change fault position”.